1. HT— 12E / HT— 12F

A. General Description —

The HT— 12E/HT— 12F are CMOS LSI designed for digit code Transmitter— Receiver System. The HT— 12E encodes 12 bits of information and serially transmits this information upon receipt of a Transmit Enable ($\overline{TE}$) signal. The HT — 12F receives the 12 bit word and interprets all 12 bits as address. When the encoder sends an address matching that of the decoder, the valid Transmission (VT) output goes high on the decoder.

B. Features —

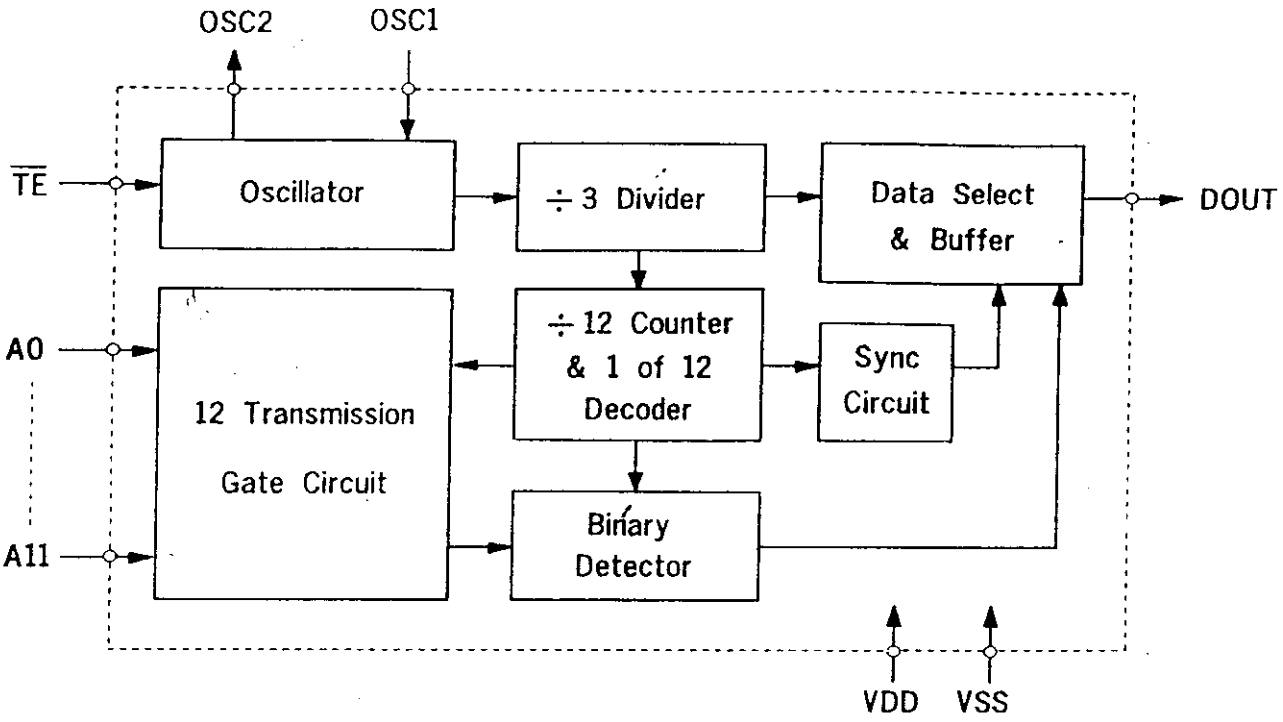
- Low power, High noise immunity CMOS technology.
- Low stand— by current: 1 uA typically .
- Wide operating voltage: 2. 4V— 12V.
- 2^{12} address code, 1 data output (VT).
- Built— in oscillator, only use 5% resistor.
- Four times transmission, Three times receive check.
- VT goes high during valid transmission.
- Easy interface with RF or Infra— Red transmission media.
- Minimum external components.
- 18 pin plastic dual— in— line package.

C. Applications —

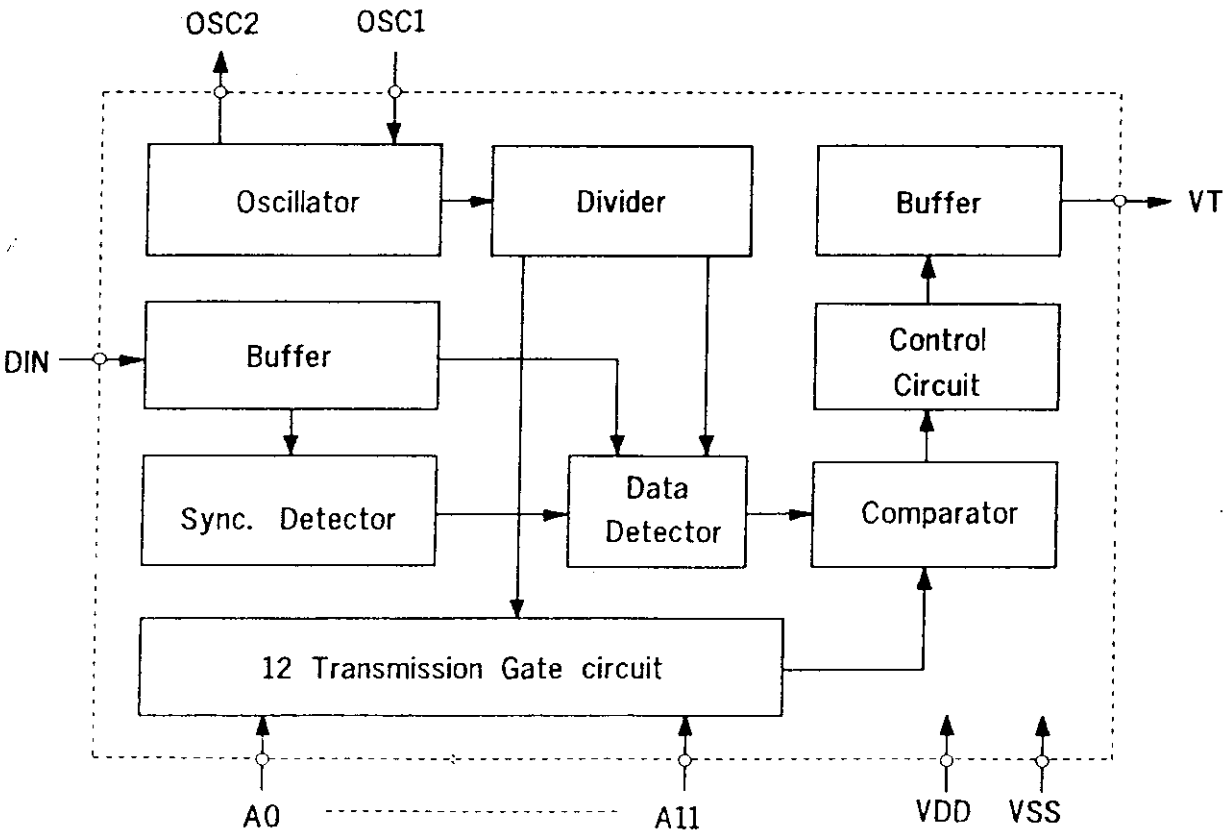
- Burglar alarm system.
- Smoke and fire alarm system.
- Garage door controller.
- Car door controller.
- Car alarm system.
- Security system.
- Cordless telephone.
- Other remote control system.

D. Block Diagram —

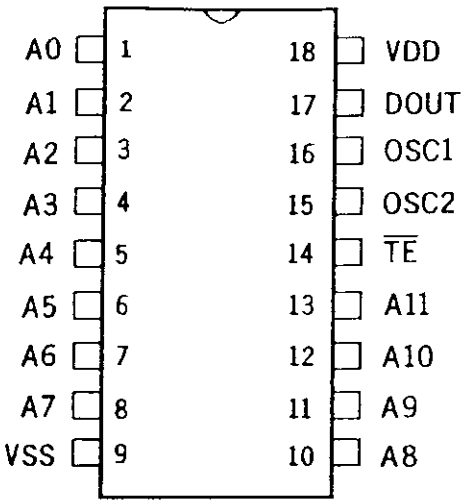
(HT— 12E)



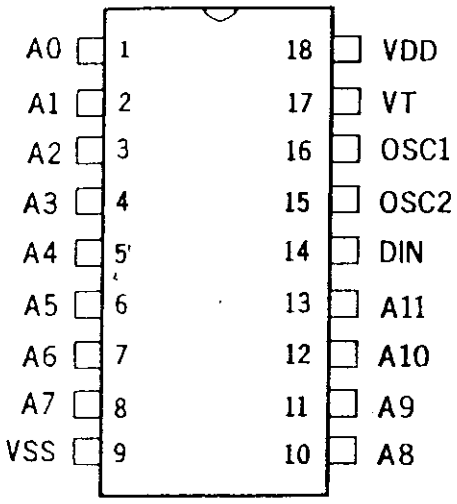
(HT— 12F)



E. Pin Assignment —



HT – 12E



HT – 12F

F. Pin Description —

(HT – 12E)

Pin No.	Pin Name	I/O	Description
1~8	A0~A7	I	Input pin for address A0~A7 setting.
9	VSS	I	Negative power supply. (GND)
10~13	A8~A11	I	Input pin for address A8~A11 setting.
14	$\overline{TE}$	I	Transmission enable.
15	OSC2	O	Oscillator output pin.
16	OSC1	I	Oscillator iutput pin.
17	DOUT	O	Encoded data output.
18	VDD	I	Positive power supply.

(HT – 12F)

Pin No.	Pin Name	I/O	Description
1~8	A0~A7	I	Input pin for address A0~A7 setting.
9	VSS	I	Negative power supply. (GND)
10~13	A8~A11	I	Input pin for address A8~A11 setting.
14	DIN	I	Data input pin.
15	OSC2	O	Oscillator output pin.
16	OSC1	I	Oscillator iutput pin.
17	VT	O	Valid Transmission indicator output, active high.
18	VDD	I	Positive power supply.

G. Absolute Maximum Ratings —

(Ta = 25 °C)

Parameter	Symbol	Minimum	Maximum	Unit
Supply Voltage	VDD	−0.3	13	V
Input Voltage	Vi	VSS −0.3	VDD+0.3	V
Storage Temperature	Tstg	−50	125	°C
Operating Temperature	Top	0	70	°C

H. Electrical Characteristics —

(Ta = 25 °C)

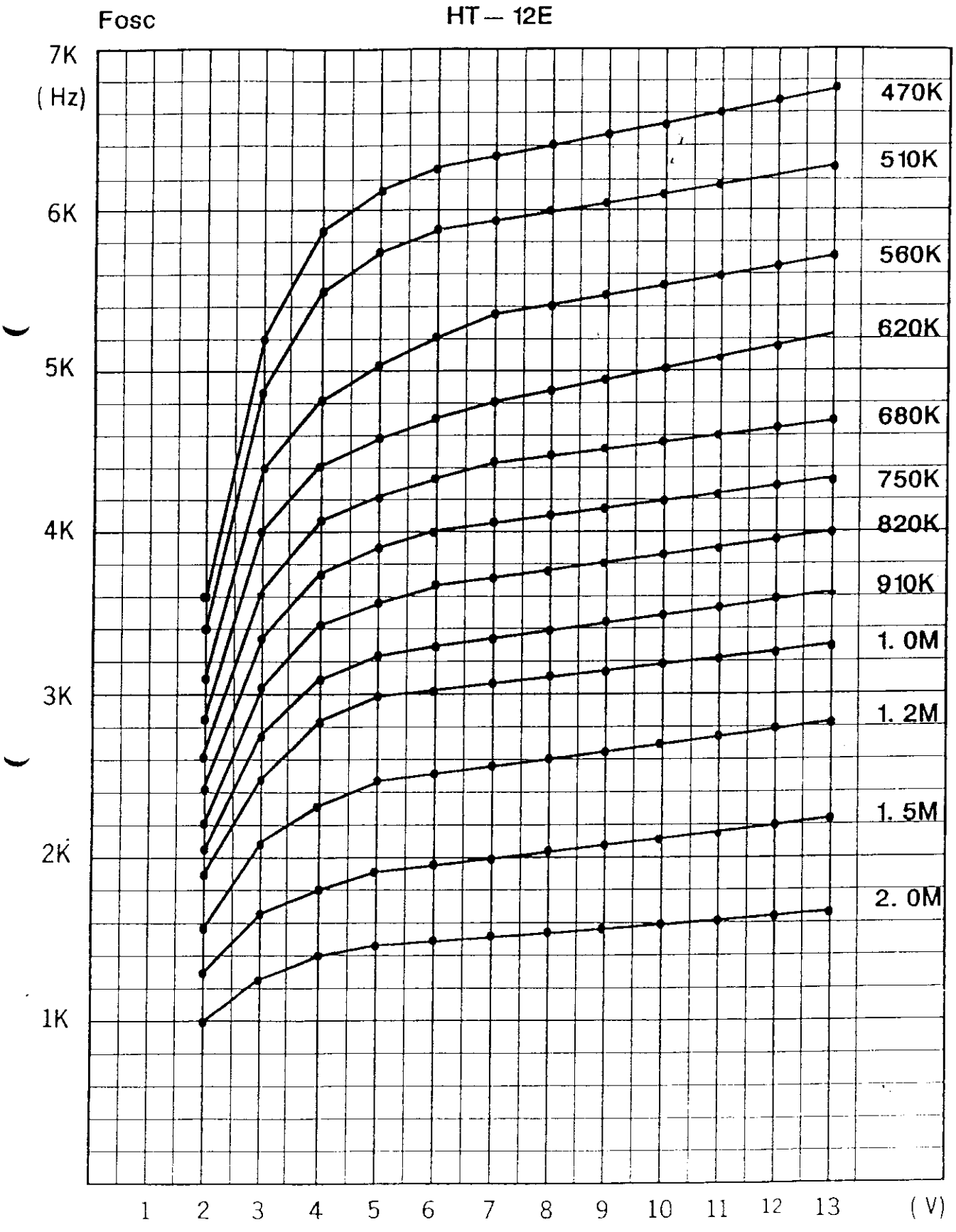
Symbol	Parameter	Test condition		Minimum	Typical	Maximum	Unit
		V_{DD}	Condition				
V_{DD}	Operating voltage			2.4	5	12	V
I_O	Output drive current (Sink or Source)	5V	V_{OH}=0.9V_{DD} (Source)	1	1.6	—	mA
		10V	V_{OL}≒0.1V_{DD} (Sink)	2	5	—	
I_{STB}	Stand−by current	3V	Oscillator stop	—	0.1	1	μA
		5V		—	0.1	1	
		10V		—	1	2	
		12V		—	2	4	
I_{DD}	Operating current No Load	5V	HT−12E Fosc=3KHz	—	40	80	μA
		10V		—	100	200	
		5V	HT−12F Fosc=200KHz	—	200	400	
		10V		—	400	800	

I. Recommended Oscillator Parameters —

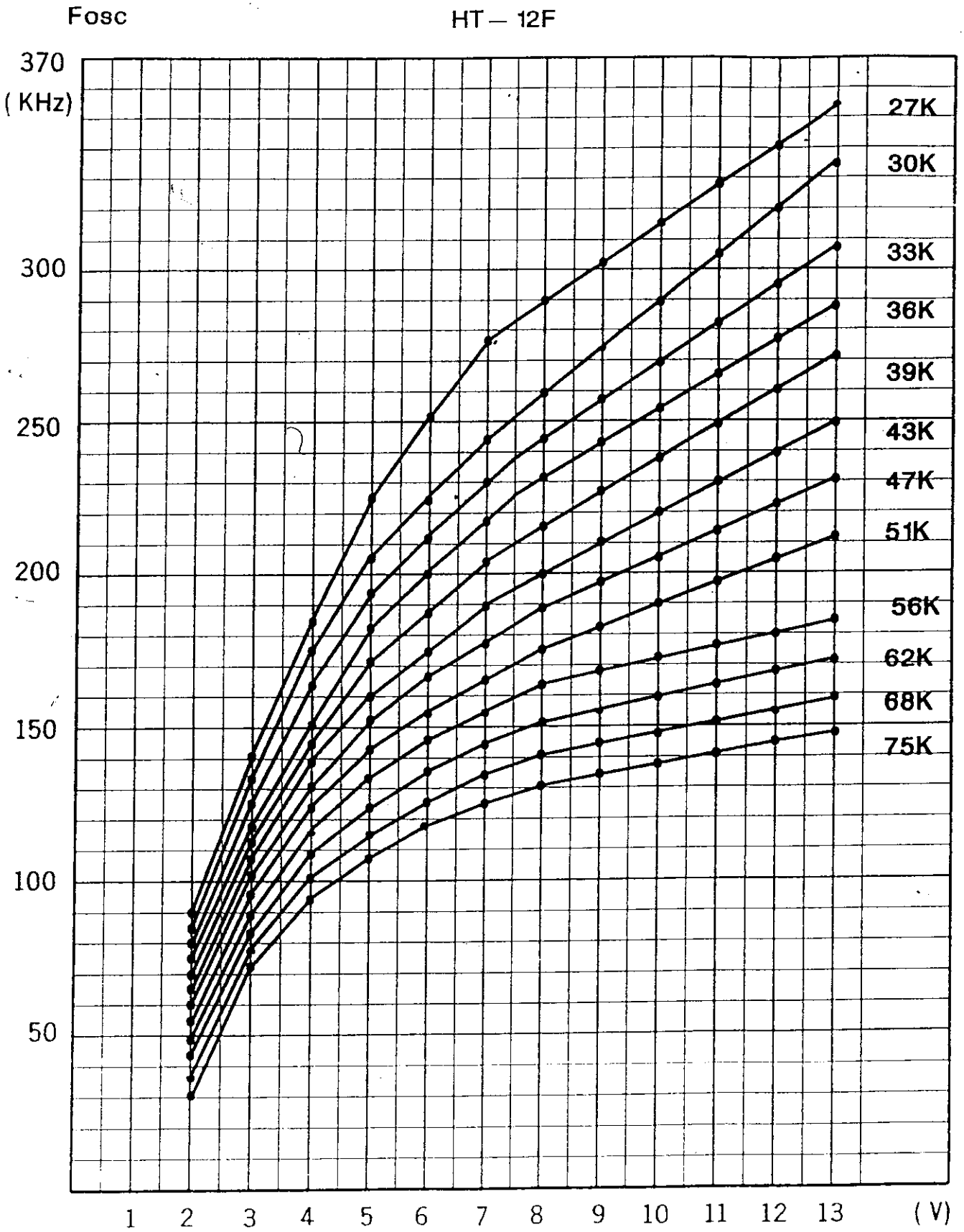
HT−12E		HT−12F	
R	Fosc	R	Fosc
1.1 MΩ	3 KHz	62 KΩ	150 KHz
750 KΩ	4.3 KHz	33 KΩ	240 KHz

Note: Recommended Fosc (HT−12F) ≒ 50 Fosc (HT−12E)

Fosc— V Curve with Rosc 470K～2.0M



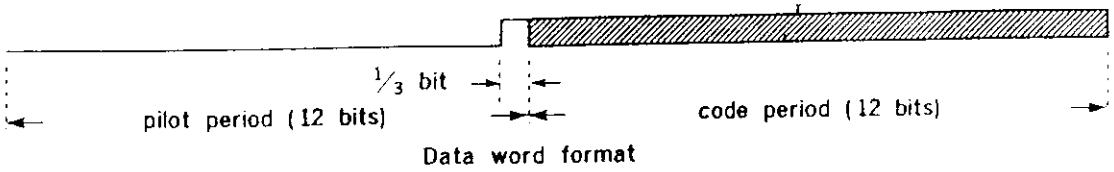
Fosc — V Curve with Rosc 75K～27K



I. Functional Description —

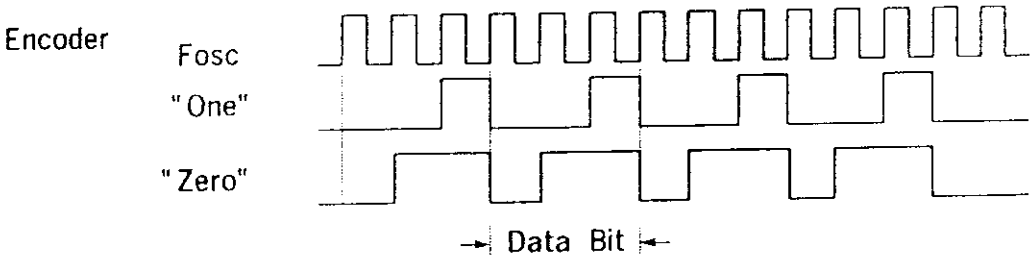
1. Encoder Operation

Upon receipt of a $\overline{TE}$ signal (active low), the HT—12E begins a 4 word transmission cycle and repeats this transmission cycle until the $\overline{TE}$ signal has been removed. One transmission cycle is composed of 4 data words each contains 2 periods: pilot and code period as shown below:

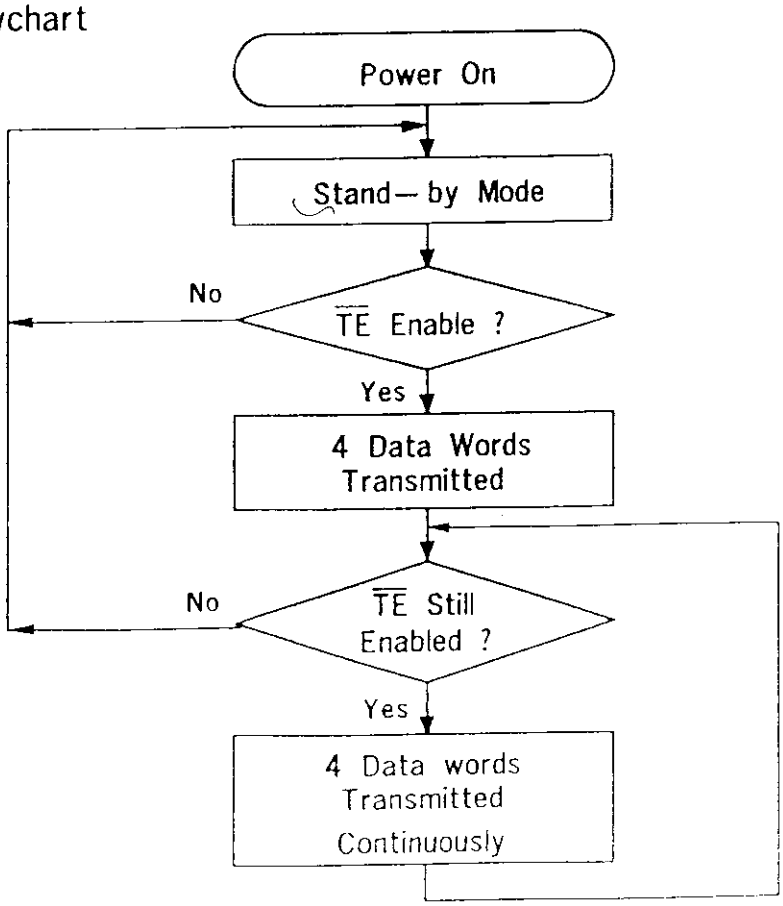


Data word format

The HT—12E detects the logic state of address (A0～A11) and transmits this information during code period. Each address pin can be set as one of two following logic state:



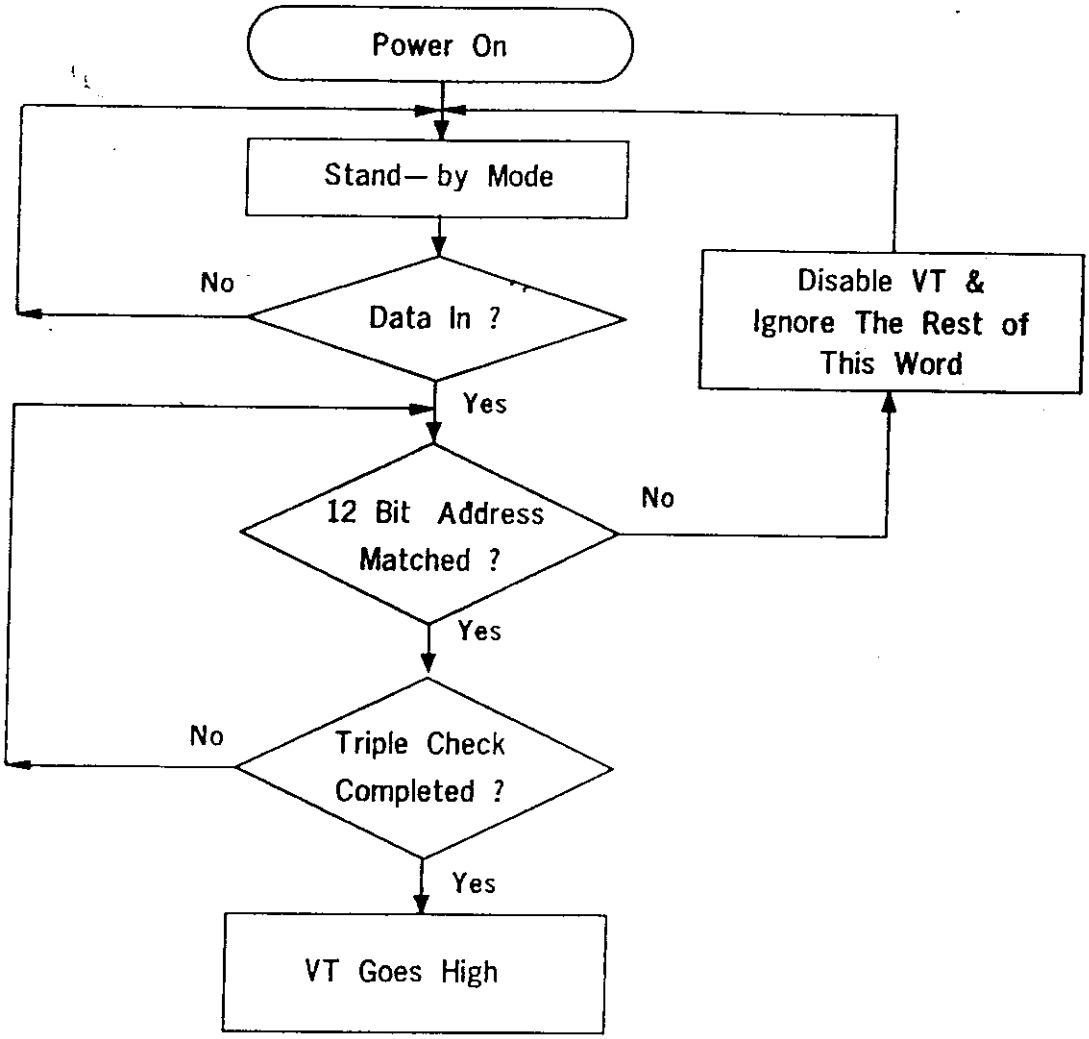
Encoder Flowchart



2. Decoder Operation

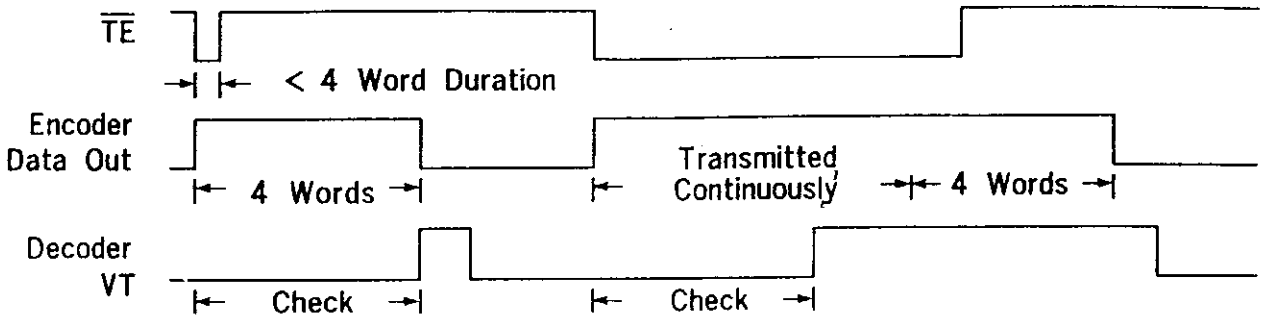
HT—12F receives the data that transmitted by HT—12E and interprets the 12 bits of code period as address and checks the received address code three times, if all the address code received match, the VT pin goes high.

Decoder Flowchart

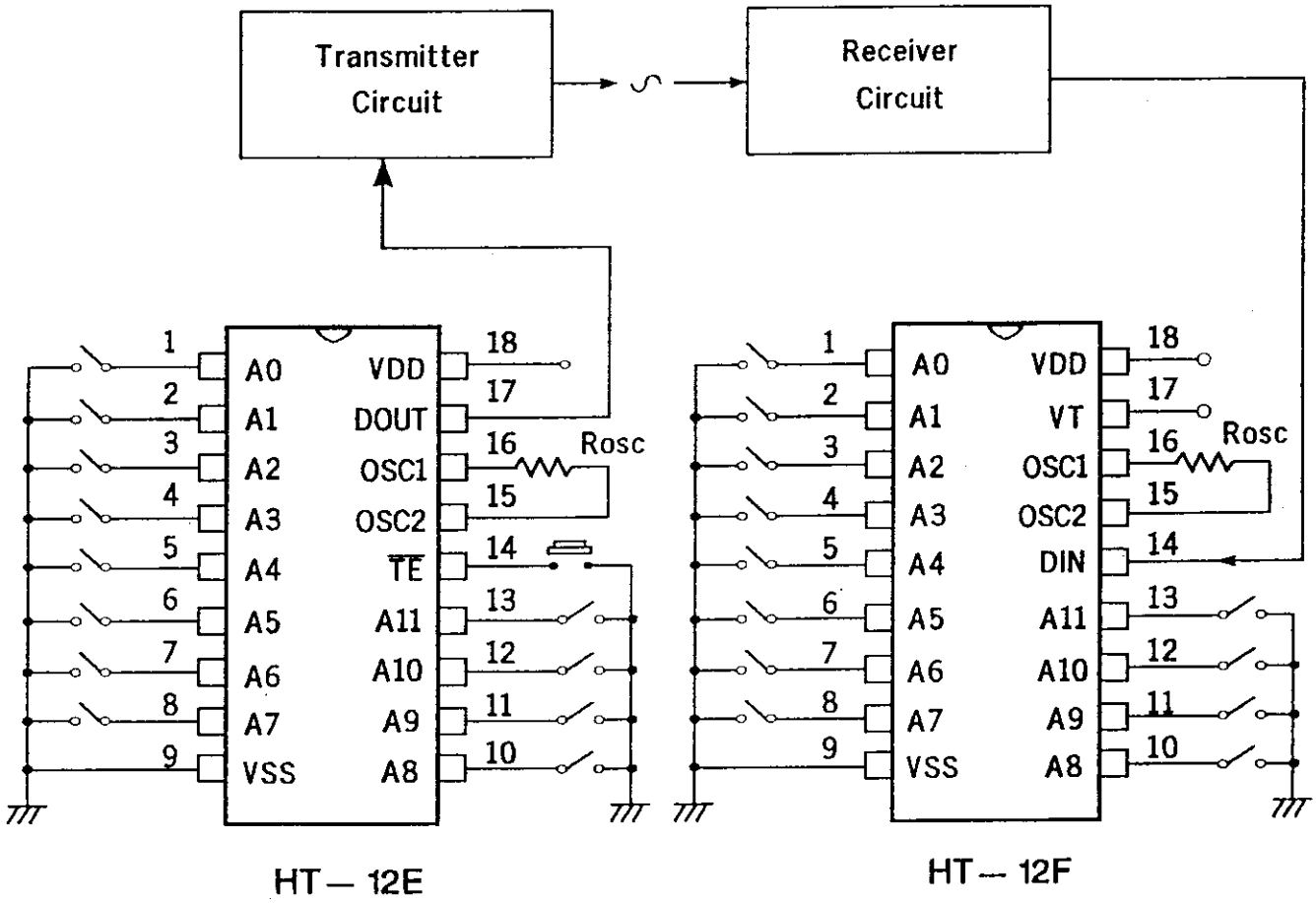


Note: The oscillator is disabled in stand—by state and activated as long as a logic 'high' signal applied to DIN pin. i. e. the DIN should be kept in logic 'low' during no signal input.

3. Encoder / Decoder



J. Application Diagram —



HT— 12E

HT— 12F