HARRIS SEMICONDUCTOR

HD-6402/883

CMOS Universal Asynchronous Receiver Transmitter (UART)

March 1997

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **8.0MHz Operating Frequency (HD-6402/883B)**
- **2.0MHz Operating Frequency (HD-6402/883R)**
- **Low Power CMOS Design**
- **Programmable Word Length, Stop Bits and Parity**
- **Automatic Data Formatting and Status Generation**
- **Compatible with Industry Standard UARTs**
- **Single +5V Power Supply**
- **CMOS/TTL Compatible Inputs**

Description

The HD-6402/883 is a CMOS UART for interfacing computers or microprocessors to an asynchronous serial data channel. The receiver converts serial start, data, parity and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity and stop bits. The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The stop bits may be one or two or one and one-half when transmitting 5-bit code.

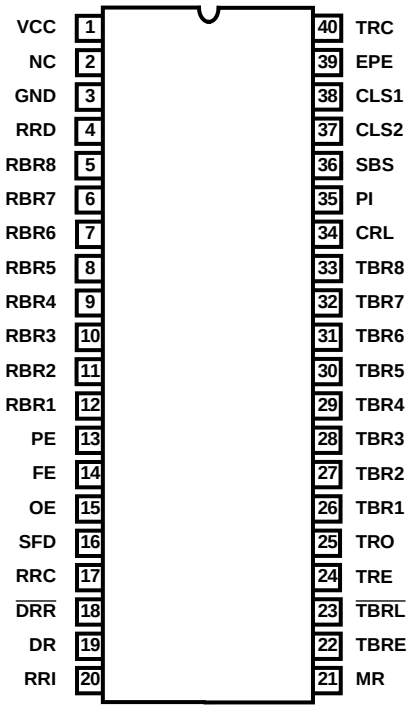
The HD-6402/883 can be used in a wide range of applications including modems, printers, peripherals and remote data acquisition systems. Utilizing the Harris advanced scaled SAJI IV CMOS process permits operation clock frequencies up to 8.0MHz (500K Baud). Power requirements, by comparison, are reduced from 300mW to 10mW. Status logic increases flexibility and simplifies the user interface.

Ordering Information

PACKAGE	TEMPERATURE RANGE	2MHz = 125K BAUD	8MHz = 500K BAUD	PKG. NO.
CERDIP	-55^{o}C to +125^{o}C	HD1-6402R/883	HD1-6402B/883	F40.6

Pinout

HD-6402/883 (CERDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **2953.1**

Control Definition

CONTROL WORD					CHARACTER FORMAT			
CLS 2	CLS 1	PI	EPE	SBS	START BIT	DATA BITS	PARITY BIT	STOP BITS
0	0	0	0	0	1	5	ODD	1
0	0	0	0	1	1	5	ODD	1.5
0	0	0	1	0	1	5	EVEN	1
0	0	0	1	1	1	5	EVEN	1.5
0	0	1	X	0	1	5	NONE	1
0	0	1	X	1	1	5	NONE	1.5
0	1	0	0	0	1	6	ODD	1
0	1	0	0	1	1	6	ODD	2
0	1	0	1	0	1	6	EVEN	1
0	1	0	1	1	1	6	EVEN	2
0	1	1	X	0	1	6	NONE	1
0	1	1	x	1	1	6	NONE	2
1	0	0	0	0	1	7	ODD	1
1	0	0	0	1	1	7	ODD	2
1	0	0	1	0	1	7	EVEN	1
1	0	0	1	1	1	7	EVEN	2
1	0	1	X	0	1	7	NONE	1
1	0	1	x	1	1	7	NONE	2
1	1	0	0	0	1	8	ODD	1
1	1	0	0	1	1	8	ODD	2
1	1	0	1	0	1	8	EVEN	1
1	1	0	1	1	1	8	EVEN	2
1	1	1	X	0	1	8	NONE	1
1	1	1	x	1	1	8	NONE	2

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage Applied . . . . . GND -0.5V to V_{CC} +0.5V
Storage Temperature Range . . . . . -65^oC to $+150^oC$
Junction Temperature . . . . . $+175^oC$
Lead Temperature (Soldering 10s) . . . . . $+300^oC$
ESD Classification . . . . . Class 1
Typical Derating Factor . . . . . 1mA/MHz Increase in ICCOP

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CERDIP Package	$50^oC/W$	$12^oC/W$

Gate Count . . . . . 1643 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55^oC to $+125^oC$

TABLE 1. HD-6402/883 D.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

D.C. PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical "1" Input Voltage	VIH	VCC = 5.5V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	2.3	-	V
Logical "0" Input Voltage	VIL	VCC = 4.5V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	0.8	V
Input Leakage Current	IID	VIN = GND or VCC, VCC = 5.5V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-1.0	1.0	µA
Logical "1" Output Voltage	VOH	IOH = -2.5mA, VCC = 4.5V (Note 1)	1, 2, 3	$-55^oC \le T_A \le +125^oC$	3.0	-	V
Logical "1" Output Voltage	VOH	IOH = -100µA VCC = 4.5V (Note 1)	1, 2, 3	$-55^oC \le T_A \le +125^oC$	VCC -0.4	-	V
Logical "0" Output Voltage	VOL	IOL = +2.5mA, VCC = 4.5V (Note 1)	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	0.4	V
Output Leakage Current	IO	VO = GND or VCC, VCC = 5.5V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-1.0	1.0	µA
Standby Supply Current	ICCSB	VIN = GND or VCC; VCC = 5.5V, Output Open	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	100	µA

TABLE 2. HD-6402/883 A.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

A.C. PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS HD-6402/883R MIN	LIMITS HD-6402/883R MAX	LIMITS HD-6402/883B MIN	LIMITS HD-6402/883B MAX	UNITS
Clock Frequency	(1) fCLOCK	VCC = 4.5V CL = 50pF	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	2.0	-	8.0	MHz
Pulse Widths, CRL, $\overline{DRR}$, $\overline{TBRL}$	(2) tPW		9, 10, 11	$-55^oC \le T_A \le +125^oC$	150	-	75	-	ns
Pulse Width MR	(3) tMR		9, 10, 11	$-55^oC \le T_A \le +125^oC$	150	-	150	-	ns
Input Data Setup Time	(4) tSET		9, 10, 11	$-55^oC \le T_A \le +125^oC$	50	-	20	-	ns
Input Data Hold Time	(5) tHOLD		9, 10, 11	$-55^oC \le T_A \le +125^oC$	60	-	20	-	ns
Output Enable Time	(6) tEN		9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	160	-	35	ns

NOTE:

1. Interchanging of force and sense conditions is permitted.
2. Tested with input levels of VIH = 2.76V and VIL = 0.4V. Rise and fall times are driven at 1ns/V.

TABLE 3. HD-6402/883 ELECTRICAL PERFORMANCE SPECIFICATIONS

A.C. PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	CIN	f = 1Mhz All Measurements are Referenced to Device GND	1	$T_A = +25^oC$	-	25.0	pF
Output Capacitance	CO		1	$T_A = +25^oC$	-	25.0	pF
Operating Supply Current	ICCOP	VCC = 5.5V, Clock Freq. = 2MHz, VIN = VCC or GND, Outputs Open	1	$-55^oC \le T_A \le +125^oC$	-	2.0	mA

NOTE:

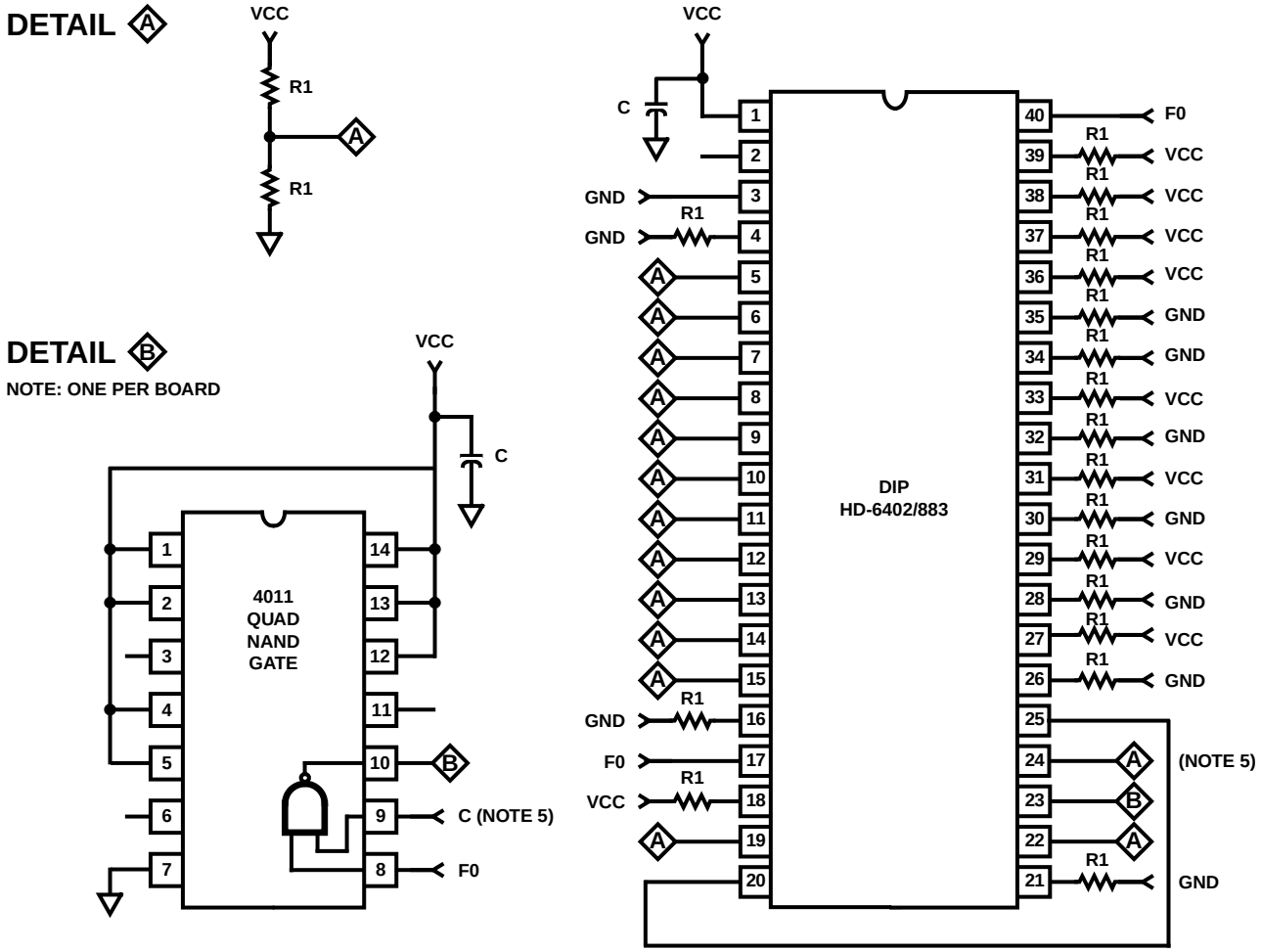
1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group C and D	Samples/5005	1, 7, 9

Burn-In Circuits

HD-6402/883 CERDIP



NOTES:

1. VCC = 5.5V ± 0.5V
2. F0 = 100kHz ± 10%
3. R1 = 47kΩ, 1/4W ± 10%
4. C = 0.01μF minimum
5. One socket per board should not be loaded, but rather have pin 24 go the “C” of the 4011.

Die Characteristics

DIE DIMENSIONS:
126.4 mils x 134.3 mils x 19 mils

METALLIZATION:
Type: Si-Al
Thickness: 10kÅ - 12kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 7kÅ - 9kÅ

WORST CASE CURRENT DENSITY:
1.42×10^5 A/cm^2

Metallization Mask Layout

HD-6402/883