# SPECIFICATIONS

## VERTICAL

| | |
|---|---|
| Bandwidth | DC to 5 MHz, ±3 dB. |
| Attenuator | 1, 2, 5 sequence, calibrated and variable. |
| Rise Time | 70 ns. |
| Overshoot | ≤5%. |
| Impedance | 1 MΩ/38 pF. |
| Sensitivity | 10 mv/cm. |

## SWEEP

| | |
|---|---|
| Type | Triggered. |
| Range | 200 ms to .2 μs in 7 steps, plus variable. |
| Trigger Source | Y1/Y2/Ext/Line. |
| Trigger Modes | AC/DC/TV; +/− Slope; Auto/Norm. |

## HORIZONTAL

| | |
|---|---|
| Sensitivity | .1 V/cm. |
| Bandwidth | DC to 1 MHz. |
| Impedance | 1 MΩ/50 pF. |
| Ext Horiz Input | X1 and X10 attenuator and variable. |

## GENERAL

| | |
|---|---|
| CRT | 5DEP31F. 8 × 10 centimeter viewing area. Blue-green, medium-persistence phosphor. 5″ round, flat face tube. |
| Accelerating Potential | Approximately 1.6 kV. |
| Graticule | Screened, 8 × 10 centimeters. |
| Power requirements | 110-130 VAC or 220-260 VAC, 50/60 Hz, 50 watts. |
| Overall Dimensions | 13″ wide, 8″ high, 17″ deep. |
| Net Weight | 15 lbs. |

# THEORY OF OPERATION

Refer to the Block Diagram (Illustration Booklet, Page 27) as you read the following material.

The dual-trace capability of this Oscilloscope allows two different signals to be displayed on a conventional CRT (cathode ray tube) that has only one set of vertical deflection plates. Two identical vertical preamplifier circuits, a switching circuit, and a vertical deflection amplifier make this possible. Each vertical preamplifier circuit attenuates its input signal by a known factor, amplifies it to a usable level, and provides the necessary positioning bias. The switching circuit (a diode-type switch), which is automatically controlled by the display control circuit, alternately allows the output signals from the two preamplifier circuits to pass to the vertical deflection amplifier. The vertical signal, a composite of both input signals, is amplified further by the vertical deflection amplifier before it is applied to the vertical deflection plates of the CRT. The signal at the vertical deflection plates, which produces the display on the CRT screen, thus represents both input signals as one "time-shared" signal.

The horizontal portion of the trace displayed on the CRT screen is produced by the sweep and trigger circuits in conjunction with the horizontal deflection amplifier. The sweep circuit produces the linear signal (ramp) used to sweep the electron beam across the CRT screen from left to right at a constant rate. This circuit is switch controlled (by the TIME/CM switch) to provide seven sweep rates needed to view and measure almost all input signals. This circuit must be triggered either by a portion of one of the vertical input signals, by an external signal, or by a portion of the line frequency signal.

In the absence of a trigger signal, an automatic baseline circuit causes the sweep circuits to operate while in the automatic mode. This ensures that, even though no signal is applied, a reference baseline (trace) will appear on the CRT screen. The sweep signal is coupled to the horizontal deflection amplifier where it is amplified before being applied to the horizontal deflection plates of the CRT. Other circuits within the horizontal amplifier also provide the necessary positioning bias.

At the end of each horizontal sweep, the blanking circuits (which are triggered by the sweep circuits) turn the trace off (blank it). This prevents a line (retrace) from being displayed as the electron beam returns to the left side of the CRT screen to start a new trace.

# CIRCUIT DESCRIPTION

Refer to the Block Diagram (Illustration Booklet, Page 27) and the Schematic (fold-in) while you read this "Circuit Description." The part numbers are arranged in the following groups to help you locate specific parts on the Schematic, circuit boards, and chassis.

| | |
|---|---|
| 1-99 | Parts on the chassis. |
| 100-199 | Parts on the vertical circuit board. |
| 200-299 | Parts on the horizontal circuit board. |
| 300-399 | Parts on the power supply circuit board. |

## VERTICAL CHANNELS

The vertical preamplifier consists of two identical circuits; one for channel Y1 and the other for channel Y2. The board-mounted components in the Channel Y1 vertical preamplifier circuit are designated by an A suffix, while those in the Channel Y2 vertical preamplifier are designated by a B suffix. (Example: A Channel Y1 divider resistor is R101A, while the corresponding divider resistor in Channel Y2 is R101B). Components without a suffix do not pertain to a specific channel. Since both channels are identical, only Channel Y1 is described in this "Circuit Description."

### INPUT CIRCUITS

When Y1 input switch SW1A (AC-GND-DC) is in the DC position, a signal applied to the Y1 input connector is coupled to the input attenuator. When the Y1 input switch is in the AC position, the signal is coupled through capacitor C1, which passes only AC signals. This permits an AC signal superimposed on a DC potential to be seen without the DC component being displayed.

The GND position of this switch disconnects the input signal and grounds the attenuator input. This allows the trace to be adjusted to a zero reference without disconnecting the test leads from the circuit under test.

Because the first, second, third, and vertical deflection amplifiers operate at a fixed gain, any signal applied to them must be within a usable range (approximately 7 mV/cm). Therefore, the primary function of the vertical input circuits is to reduce the input signal by a known factor to this usable level.

The vertical input circuit basically consists of a high impedance attenuator, an input follower, and a low impedance attenuator. These circuits function together, through VOLTS/CM switch (SW2), to provide the total desired attenuation. The attenuator obtains its four attenuation factors (1, 10, 100, and 1000) from four divider networks (resistors R101A through R104A, and capacitors C103A through C107A). At DC and low AC frequencies, the resistive dividers reduce the input signal level. At higher frequencies, however, attenuation is determined by the resistor-capacitor (RC) networks.

Trimmer capacitors C103A, C104A, and C106A are used to adjust the capacitor division ratio to match the resistor ratio. Trimmer capacitors C101A and C102A

are adjusted during calibration to make the input capacitance of the Oscilloscope equal in all positions of the VOLTS/CM switch. This is essential when an attenuation probe (usually ×10) is used. Resistors R1A, R2A, and R106A are used to suppress oscillations in the attenuator circuit.

The input follower circuit consists of an FET (field-effect-transistor) source follower and DC current source. The attenuated input signal is coupled through resistors R106A and R107A and capacitor C108A to the gate of FET source follower Q101A-1. Capacitor C108A forms a high frequency path around R107A for improved frequency response. Input protection is provided by the two diodes D101A and D102A. The diodes are connected to the plus (+) and minus (−) 8-volt supplies. Thus, if the signal at the junction of the two diodes exceeds 8 volts, the diodes become forward biased and clamp the signal to a level that is within a diode drop of 8 volts. This prevents damage to Q101A if the VOLTS/CM switch is in a low range, and a high potential is applied to the input.

Transistor Q101A-1 provides a match between the high impedance of the input attenuator and the low impedance of the second attenuator. Transistor Q101A-2 is used as a constant current source. DC Balance control R112A sets the current through Q101A-2 so the voltage at the drain is 0 volt when no signal is present at input J1. Capacitor C112A forms a high frequency path around resistor R107A for improved high frequency response.

The output from Q101A-1 is coupled to the low impedance attenuator through variable attenuator control R3. The low impedance attenuator attenuates in a 1, 2, 5 sequence from the three divider resistors (R115A, R116A, and R117A).

The output from the second attenuator is coupled to the gate of transistor Q102A-1. Q102A-1 and Q102A-2 form the first gain stage with a gain factor of about 3. Vertical Position control R4A is connected to the gate of transistor Q102A-2. Transistor Q103A, a constant current source for the stage, and Bias Adjust control R138A sets the current through the stage. This in turn sets the bias voltage at the drain of transistors Q102A-1 and Q102A-2.

The output of the first gain stage is direct-coupled to the second gain stage through resistors R124A and R131A. The second stage is made up of transistors Q104A and Q105A. The gain factor of this stage is about 10. Vertical Calibration control R143A sets the gain of this stage and also of the vertical amplifier.

The output of the second stage is coupled to the third gain stage through resistors R157A and R158A. The gain of the third stage is about 10. The signal at the emitter of the second gain stage is coupled to the trigger amplifier through resistors R142A and R145A. The trigger amplifier will be described later.

## DIODE SWITCH

Both preamplifier circuits (channels Y1 and Y2) share the vertical deflection amplifier. This is accomplished with two high-speed diode switch networks (D108A through D112A and D108B through D112B) that are actuated by the display control circuit. When one diode switch is turned on, the other is turned off, so only one signal can be coupled to the vertical deflection amplifier. Two-channel operation is accomplished by turning each diode switch network on and off at a rapid rate or on alternate display sweeps. Control of the diode switch will be described in a later section.

## VERTICAL DEFLECTION

From the diode switch, the input signal is direct-coupled to the vertical deflection amplifier through resistors R166 and R168. This amplifier (made up of transistors Q113, Q114, Q115, and Q116) is wired in a differential cascode configuration, with a gain of about 20. Capacitor C121 between the emitters of Q113 and Q114 provides high-frequency square wave compensation. Ferrite beads on the base leads of common-base amplifier Q115/Q116 prevent oscillations in the amplifier. Circuit loading is provided by resistors R177 and R178. The output of this amplifier is coupled to the vertical deflection plates of the CRT for beam control. Vertical beam deflection requires between 9 and 12 voltsc/cm, depending on individual CRT characters.

### TRIGGER AMPLIFIER

A differential amplifier and follower make up the trigger amplifier circuit. Its output is used to supply a trigger signal to the trigger circuit.

A portion of the input signal is coupled from the emitters of Q104A/Q105A to the input of differential amplifier Q106/Q107 in the trigger amplifier circuit. Emitter follower Q109A couples the trigger signal from the inverting leg (collector of Q108A) of the differential amplifier to the trigger circuit. Transistor Q108A is a temperature-compensated constant current source for this circuit. Trigger Zero control R152A in the emitter leg adjusts the current so the output of the follower will be zero with no signal to the trigger amplifier. Thus, the circuit performs as a differential to single-ended converter.

### CONTROL CIRCUIT

The control circuit consists of the two switch driver transistors Q117 and Q118, the control integrated circuit U102, sections A and B of integrated circuit U101 making up the chopper oscillator, and Vertical Mode switch SW4. Section C of U101 acts as an inverter/buffer and supplies the chopper blanking signal.

When single trace operation is desired, switch SW3 is placed either in the Y1 or Y2 position. In these positions, integrated circuit U102 selects the proper switch driver transistor to allow the selected channel to operate. When the chop mode of the dual trace operation is desired, switch SW3 is placed in the Chop position. The chopper oscillator is activated and it applies a 200 kHz toggle pulse to pin 12 of U102. U102 drives the switch driver transistors at a 100 kHz rate. Thus, the two channels are switched on and off at this rate. Pictorial 10-1 (Page 112) shows a typical, 2-trace, chopped display that has been magnified for clarity. The oscillator signal is also applied to the blanking amplifier ("S" on the power supply circuit board) by section C of U101. This signal blanks the CRT during each on/off transition of the two channels. It is also desirable to switch the oscillator off during the retrace time. Therefore, a pulse is coupled from sweep control integrated circuit U201B to chopper oscillator U101A/U101B and control integrated circuit U102 to inhibit any switching during this time.

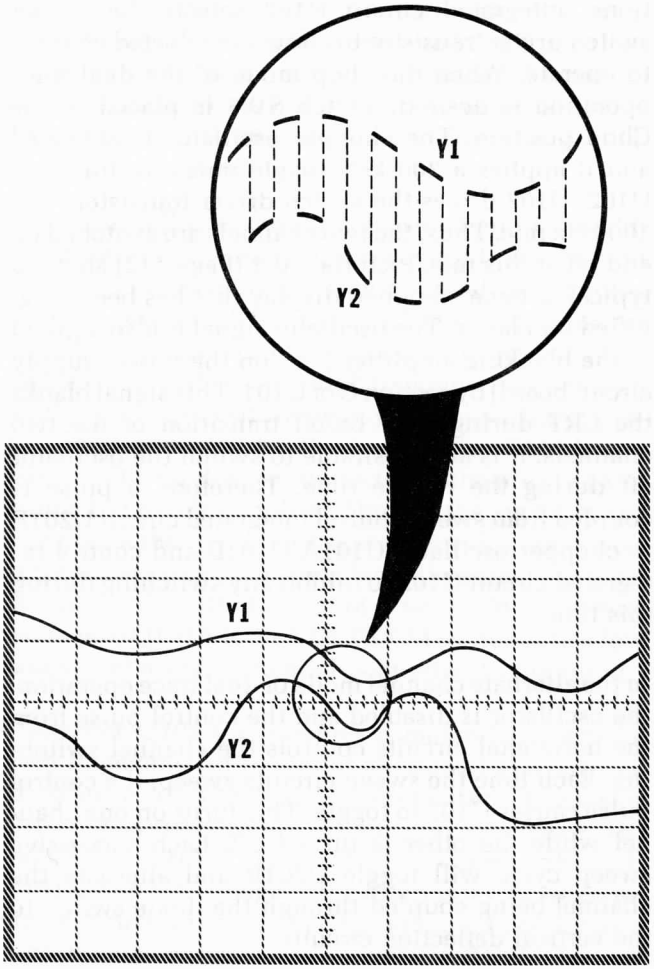
In the alternate channel mode of dual trace operation, the oscillator is disabled and the control pulse from the horizontal circuits controls the channel switching. Each time the sweep circuits sweep, the control pulse causes U102 to toggle. This turns on one channel while the other is turned off. Each successive sweep cycle will toggle U201B and alternate the channel being coupled through the diode switch to the vertical deflection circuits.

## TRIGGER AND SWEEP CIRCUITS

On command from a trigger pulse, the horizontal time base circuits generate a linear ramp signal (sweep) to drive the CRT horizontal deflection plates and move the dot across the screen at a constant rate. In the automatic triggering mode, if no trigger is present, the time base circuits free-run and generate an auto baseline.

When a trigger signal of sufficient amplitude is present, the trigger amplifier amplifies the signal and presents it to the trigger comparator through the slope switch. The output of the comparator changes state and turns on the sweep control and allows the timing capacitor to be charged through the "bootstrap" constant current source. The charging of the capacitor produces a linear ramp signal that is coupled through the voltage followers to the horizontal deflection circuits.

The ramp signal is also coupled to the sweep end circuit. When the ramp reaches a preset voltage level, set by the Sweep Length control, the sweep end circuit triggers the blanking flip-flop and ramp hold-off monostable.




**PICTORIAL 10-1**

## TRIGGER

In the automatic triggering mode, the trigger circuit examines the trigger signal for a proper trigger point. If the signal is large enough, the sweep circuit is activated by the trigger. If the signal is insufficient or absent, the circuits are allowed to free run.

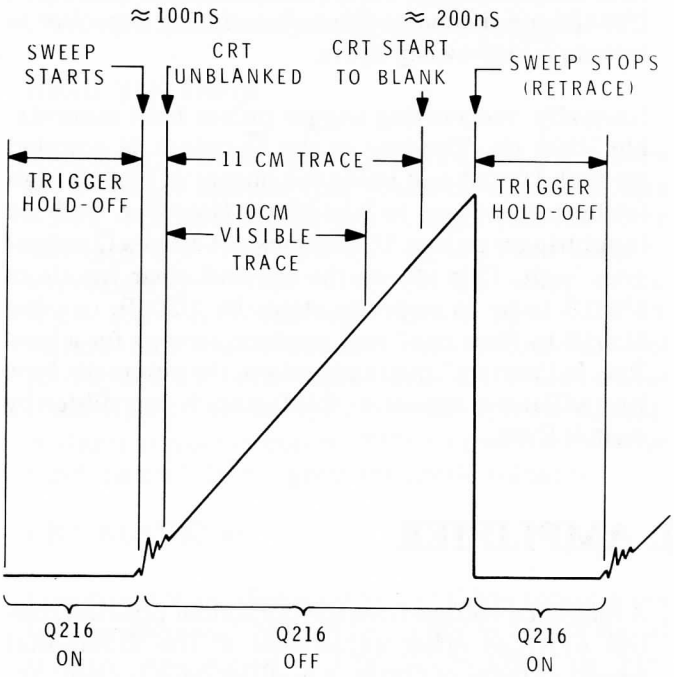
Depending on the desired trigger mode, one of four sources can be selected by the Trigger switch: Channel Y1 Trigger, Channel Y2 Trigger, External Trigger, or Line Sync. The Channels Y1 and Y2 trigger signals are provided by the vertical preamplifier trigger circuits, while the line sync signal is tapped directly off the 1-volt transformer winding. The external trigger input signal is coupled directly to trigger switch SW4. The signal is then coupled to switch SW6. SW6 selects the type of coupling (AC, DC, or TV) that will be used to couple the signal to the trigger circuits. In the AC position, the signal is coupled through capacitor C201 to the trigger circuits. In the DC position, the signal is coupled direct, and in the TV position, the signal is coupled through capacitors C201, C202, resistor R201, and diode D201. The circuit composed of capacitor C202, resistor R201, and diode D201 forms a low-pass filter and DC restorer. This circuit allows the trigger circuits to be synchronized to the vertical frame rate of a complex video TV signal.

The trigger signal is coupled to the first gain stage through resistor R252 and capacitor C229. C229 forms a high frequency path around R252 for high frequency response. Resistor R280 sets the input impedance of the amplifier. Diode D214 and the gate-drain junction of Q201A provide input protection.

The first gain stage is made up of transistors Q201A and Q201B. Transistor Q202 is a constant current source for the stage. Trigger Balance control R211 adjusts the current through the stage and the bias voltage at the output of the trigger amplifier. Trigger Level control R7 is connected to the gate of transistor Q201B.

The second gain stage is formed by transistors Q203 and Q204 and has a gain of about 30. The output of this stage is coupled to emitter followers Q205 and Q206. The output of the emitter followers is connected to Slope switch SW7.

The amplified signal, with either positive or negative slope as selected by SW7, is coupled to pin 1 of integrated circuit U202A. U202 contains four Schmitt input gates. A trailing edge or low-going pulse applied to pin 1 of U202A causes the output to go high. This high is coupled to pin 11 of U201B and to pin 3 and 4 of U203. U201B controls the sweep circuits and U203 controls the auto baseline portion of the sweep circuits.




**PICTORIAL 10-2**

## SWEEP

The negative edge of the trigger pulse activates U201B and turns transistor Q216 off. This lets the timing capacitor charge through the bootstrap current source, and generates a linear voltage ramp. The ramp (sweep signal) is coupled to the horizontal deflection circuit, and the remaining sweep circuits. When the ramp reaches a pre-determined level, the CRT is blanked, U201B is reset, and Q216 is turned on to provide a discharge path for the timing capacitor (ramp returns to the zero level).

Refer to Pictorial 10-2 for the following discussion.

When transistor Q216 turns off, the timing capacitor begins to charge. After about 100 nS, the CRT unblanks and the trace becomes visible. This short delay hides any switching transients. At a preset ramp level, the CRT is again blanked before the trace is stopped (to give the CRT time to fully blank). After the short delay, transistor Q216 is turned on and the timing capacitor is discharged.

Initially, sweep control U201B is in a reset condition (Q is low and $\overline{Q}$ is high) and transistor Q216 is turned on. A trigger pulse from U202A will toggle U201B and switch Q high and $\overline{Q}$ low. The low from $\overline{Q}$ turns transistor Q216 off and toggles blanking control U201A. As Q216 turns off, the timing capacitor begins to charge through the "bootstrap" current source. At the same time, U201A switches the CRT blanking circuit and unblanks the CRT.

The bootstrap current source is part of the sweep generator. Field effect transistors Q207A and Q207B, and transistor Q217 form a voltage follower with a gain of approximately 1. It has a very high input impedance to prevent circuit loading, which could cause a non-linear voltage ramp (sweep). The junction of resistors R233 and R10 is held to a level 10 volts above the output of the emitter follower by zener diode D205. Since the follower input voltage equals the output voltage, the voltage across the selected timing resistor (R223, R224, R225, or R226) will always be constant. This will produce a constant current to charge the selected timing capacitor (C215, or C216). When variable control R10 is turned from its CAL position, the voltage differential is lowered. Thus, the charging current will be reduced and as a result, the sweep speed is reduced. The Variable control is used to provide continuous sweep speeds between the calibrated ranges. Zero ADJ control R231 adjusts the follower for the proper voltage offset.

The output of the sweep generator is coupled through resistor divider R272 and R273 to the horizontal deflection amplifier. It is also coupled through Sweep Length control R236 to Schmitt gate U204B. Control R236 is adjusted so the output of the Schmitt trigger-type gate will go low when the ramp voltage exceeds approximately 1.8 volts. (This represents a horizontal sweep of about 11 centimeters.) The low from U204B resets (clears) blanking control U201A, which blanks the CRT. Zener diode D206 protects the Schmitt trigger from misalignment or malfunction of the sweep generator. The function U204A will be described later.

The low from sweep end gate U204B is coupled to hold-off monostable U205. This signal is coupled via resistor R228 and capacitor C214. This RC combination causes a small delay that insures that the retrace will not occur until after the CRT is blanked. The hold-off monostable toggles ($\overline{Q}$ goes low) and remains in this condition until it "times out." The hold-off time is determined by TIME/CM switch SW5C and is of sufficient duration to insure complete retrace. With pin 13 of U202D high (from U204A), the low from $\overline{Q}$ of U205 will force pin 11 of U202D high. Pins 9 and 10 of U202C will go high and pin 8 of U202C is forced low resetting sweep control U201B. This forces the $\overline{Q}$ output high and turns on Q216 which quickly discharges

the sweep timing capacitor (retrace). The low from pin 8 of U202C does not affect gate U202B because pin 5 of U202B is already low (auto-baseline monostable U203 toggled by trigger signal). The low from hold-off monostable U205 "locks up" sweep control U201B, so that it cannot toggle on a trigger signal until after hold-off. After U205 "times out," U201B can toggle on the next trigger signal and start a new cycle.

If, for any reason the sweep control circuitry should "hang up," such as at initial turn-on, the ramp voltage would continue to increase. A voltage level would be reached where anti-lockup control U204A would activate and (through U202D and U202C) reset (clear) U201B, and discharge the sweep timing capacitor to initiate a new sweep cycle.

Normally, reoccurring trigger pulses hold monostable U203 on. The low at the $\overline{Q}$ output is coupled through U202B and holds the output of U202B high for normal sweeps to take place. However, with no input trigger pulses, U203 times out and its $\overline{Q}$ output goes high. This allows the set and clear inputs of U201B to be in opposite states by U202B, causing U201B to "free run" and produce sweeps for a base line. In "normal" mode operation, the automatic base line will never appear, as this feature is overridden by switch SW8.

# HORIZONTAL AMPLIFIER

The sweep signal is coupled to the gate of Q208A by resistor R239 and capacitor C218. C218 forms a high frequency path around R239 for high frequency improvement. Resistor R240 sets the input impedance to the amplifier. Input protection is provided by diode D209 and the gate-drain junction of Q208A, connected to the ±9-volt sources; thus, clamping the input signal to these potentials. Transistor Q208A is connected as a source follower. Transistor Q208B is connected as current source for Q208A. Control R247 sets the current through this stage. The signal is connected from the drain of Q208B to the base of Q209. When the horizontal amplifier is used in the external/horizontal mode of operation, the input of the amplifier is connected to the X1 and the X10 attenuator. The attenuator is formed by resistors R242 and R243. Capacitors C219 and C220 provide frequency compensation. External horizontal variable control R11 and resistor R286 are also switched in at this time.

A reference voltage from the horizontal position control provides offset adjustment at the differential amplifier (base of Q210). Amplifier gain is about 10. Control R251 adjusts the gain of this amplifier, and therefore, the overall gain of the horizontal deflection circuit. This is to compensate for the individual deflection characteristics of the CRT. Transistor Q211 is the constant current source for this amplifier section. Control R257 adjusts the current through this stage and thus the bias voltage at the collectors of Q209 and Q210.

Final amplification occurs in the third deflection amplifier. It is a cascode differential amplifier with a gain of about 25. The output is coupled to the horizontal deflection plates of the CRT for beam control. Horizontal beam deflection requires between 14 and 20 volts/cm, depending on individual CRT characteristics.

# POWER SUPPLIES AND BLANKING

## +130 AND +160 VOLTS

Full-wave bridge rectifier diodes D307, D308, D309, and D310 produce 170 volts which is reduced to provide the +160-volt supply used in the horizontal deflection amplifier. A second filter divides the 160-volt source down to +130 volts for the vertical deflection amplifier, the blanking amplifier, and the astigmatism control.

## ±9 AND +5 VOLTS

Diodes D303, D304, D305, and D306 comprise two full-wave rectifiers that produce positive and negative 15 volts DC from the power transformer. These voltages are filtered and then coupled to voltage regulators U301, U302, and U303. Regulators U303 (−9 V) and U302 (+9 V) are connected in a tracking con-

figuration by resistors R334, R335, and R336. If one regulator shuts down, the other one is also shut down. U301 provides the regulated +5 volts supply.

## HIGH VOLTAGE

Diodes D301, D302 and capacitors C301, C302 make up a voltage doubler that produces approximately −2000 VDC at nominal line voltage. Resistor R301 and capacitor C303 filter and reduce the voltage to approximately −1650 VDC. Divider string D311, R308, R17, R6, R309, and R310 supply the CRT cathode bias and a reduced voltage for focus control R6. Capacitor C320 bypasses diode D311 and resistor R338. Resistor R338 limits the CRT cathode current. Astigmatism adjust control R330 and emitter follower Q307 control the astigmatism anode voltage.

## CRT BLANKING

Free-running oscillator Q305 and Q304 controls the trace brightness. The high frequency oscillator signal is capacitor-coupled to a bridge rectifier that produces a DC voltage on the cathode to turn on the CRT. The amplitude of the oscillator signal (controlled by the blanking circuit) can be increased or decreased by changing DC levels, or decreased by pulses. An oscillator signal of larger amplitude (as adjusted by the Intensity or Bias Adjust controls) will produce a larger DC voltage on the CRT cathode, which will make the trace brighter. A retrace pulse will reduce the amplitude of the oscillator signal, and the resulting reduced DC voltage will turn off the CRT during "retrace" or "hold-off."

To fully understand the blanking circuits, keep the following three ideas in mind.

1. The CRT is blanked when the control grid is 82 volts **more negative** than the cathode.

2. As the 82-volt difference between the grid and the cathode is reduced, the CRT is unblanked and the beam intensity is increased.

3. The CRT must be blanked and unblanked when the sweep circuits are operating, and there must be spot control when the Oscilloscope is used in the external horizontal mode. Therefore, there must be two paths of control: an AC path and a DC path.

The blanking amplifier provides the necessary gain to amplify the input blanking pulses and the voltage from the Intensity control. The Intensity control controls the output DC level of the amplifier (emitter of Q306), and the input blanking pulses reduce this DC level for the duration of each pulse. The leading and trailing edges of the amplified blanking pulses are capacitor-coupled to the grid of the CRT by C315 and R325.

At slow sweep speeds, the CRT is blanked for a very long period of time, or not at all in the EXT Horizontal position. Because of this, a "DC restoration" scheme is needed to translate the DC level at the output of the blanking amplifier to the control grid of the CRT. This is done by amplitude modulating an oscillator (Q305 and Q304) that is capacitor coupled by C314 to demodulator diodes D316 and D320. The demodulator is referenced to the −1650 volt supply and the output is coupled to the CRT control grid by R324 and R325.

The amplitude of the oscillator output follows the DC output of the blanking amplifier on a 1:1 basis. Then the output of the demodulator follows the peak value of the oscillator waveform. This means, then, that the DC output of the blanking amplifier is translated to the CRT grid on a 1:1 basis.

The blanking amplifier has a common base input stage, Q301. Here, the input blanking pulses and the Intensity control voltage are summed in its emitter. Transistors Q302, Q303, and Q306 are current and voltage amplifiers whose gain is determined by the ratio of feedback resistor R318 and the appropriate input resistance. Capacitor C312 is for high frequency compensation.

The blanking amplifier is coupled to the emitter of Q304 by R329. Q304, and Q305 form an emitter-coupled oscillator. Capacitor C319 and emitter resistor R333 determine the frequency of oscillation, which is approximately 200 kHz. Diode D319 protects Q304 from negative spikes during turn-on when C314 charges. D318 is referenced to a maximum voltage that the oscillator is limited to and clamps the output of the oscillator if it tries to exceed this voltage. The reference voltage is set by resistors R326 and R327, and C317 filters this voltage.

## CALIBRATOR

The calibrator section consists of resistor R307 and diodes D312 and D313. The resistor and the diodes clamp the voltage to jack J3 to approximately .94 volt peak to peak.